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EXAMINER	
KRAIG, WILLIAM F	

ART UNIT	PAPER NUMBER
2892	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/759,081	LI, CHOU H.	
	Examiner	Art Unit	
	WILLIAM F. KRAIG	2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 November 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *See Continuation Sheet* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5,6,8,10,15,16,18-20,22-26,28,30-34,36,38,45-50,52-54,56-74 and 76-85* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continuation of Disposition of Claims: Claims pending in the application are 1,3,5,6,8,10,15,16,18-20,22-26,28,30-34,36,38,45-50,52-54,56-74 and 76-85.

DETAILED ACTION

Priority

1. Applicant's claim for the benefit of a prior-filed application under 35 U.S.C. 119(e) or under 35 U.S.C. 120, 121, or 365(c) is acknowledged. Applicant has not complied with one or more conditions for receiving the benefit of an earlier filing date under 35 U.S.C. 120 as follows:

The benefit claims filed on 11/23/2007 (and previously filed on 03/16/2006) was not entered because the required references were not timely filed within the time period set forth in 37 CFR 1.78(a)(2) or (a)(5). If the application is an application filed under 35 U.S.C. 111(a) on or after November 29, 2000, the reference to the prior application must be submitted during the pendency of the application and within the later of four months from the actual filing date of the application or sixteen months from the filing date of the prior application. If the application is a nonprovisional application which entered the national stage from an international application filed on or after November 29, 2000, after compliance with 35 U.S.C. 371, the reference to the prior application must be made during the pendency of the application and within the later of four months from the date on which the national stage commenced under 35 U.S.C. 371(b) or (f) or sixteen months from the filing date of the prior application. See 37 CFR 1.78(a)(2)(ii) and (a)(5)(ii). If applicant desires the benefit under 35 U.S.C. 120 based upon a previously filed application, applicant must file a petition for an unintentionally delayed benefit claim under 37 CFR 1.78(a)(3) or (a)(6). The petition must be accompanied by: (1) the reference required by 35 U.S.C. 120 or 119(e) and 37 CFR 1.78(a)(2) or (a)(5)

to the prior application (unless previously submitted); (2) a surcharge under 37 CFR 1.17(t); and (3) a statement that the entire delay between the date the claim was due under 37 CFR 1.78(a)(2) or (a)(5) and the date the claim was filed was unintentional. The Director may require additional information where there is a question whether the delay was unintentional. The petition should be addressed to: Mail Stop Petition, Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Double Patenting

2. The nonstatutory double patenting rejection of claims 1, 3, 5, 6, 8, 10, 15, 16, 18-20, 22-26, 28, 30-34, 36, 38, 45-50, 52-54 and 56-85 is withdrawn in light of Applicant's amendments to the claims dated 11/23/2007.

Claim Objections

3. Claim 15 is objected to because of the following informalities: The word --the-- should be inserted between "of" and "top" on line 2 of the claim.

4. Claims 19, 47, 49 50, 58 and 85 are objected to because of the following informalities: There are spaces in these claims that should be removed. For instance, there is a space after the word "dielectric" on line 7 of claim 19, a space after the word "signal-" on line 3 of claim 47, and a space after the word "selected" on line 4 of claim 49.

5. Claim 20 is objected to because of the following informalities: The word "orders" should be replaced by --order-- (Line 13).

6. Claim 38 is objected to because of the following informalities: The word "dialectical" should be replaced by --dielectrical-- on line 7 of the claim, and the word --a-- should be inserted between "and" and "mixture" on the last line of the claim.

7. Claim 56 is objected to because of the following informalities: The claim should be dependent from claim 52, not from claim 1.

8. Claim 58 is objected to because of the following informalities: The semicolon at the end of line 13 of the claim should be replaced by a comma.

9. Claim 63 is objected to because of the following informalities: The limitations "bottoms as in" and "of Peltzer and Murphy devices" should be removed from the claim.

10. Claim 73 is objected to because of the following informalities: The limitation "sad" should be replaced by --said-- on line 18 of the claim.

11. Claims 78 and 79 are objected to because of the following informalities: The limitations "a top and a bottom major surfaces", and "a bottom major surfaces" should be replaced with --a top major surface and a bottom major surface-- and --a bottom major surface--, respectively.

12. Claim 80 is objected to because of the following informalities: The limitations "a selected top and a selected bottom major surfaces", and "a selected bottom major surfaces" should be replaced with --a selected top major surface and a selected bottom major surface-- and --a selected bottom major surface--, respectively.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

The following is a quotation of the second paragraph of 35 U.S.C. § 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

13. Claims 3, 19, 23, 38 and 60 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Regarding claims 3 and 23, the claims to the solid material pocket and the semiconductor material body having a specified vertical thickness of less than a few hundred atomic layers are not disclosed in the specification. Instead the specification relates that the dimensions have an *accuracy* of or better than a few hundred atomic layers, not that the actual dimensions are of a few hundred atomic layers.

Regarding claims 19, 38 and 60, the claims to the solid state material region, solid state material body and device material region consisting essentially of a "non-semiconductor" are not disclosed in the specification.

14. Claims 56 and 71 are rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 56 (as currently amended) contains the limitation "said two solid material pockets". There is insufficient antecedent basis in the claim (including the limitations of claim 1, from which claim 56 depends) for this limitation.

Claim 71 (as currently amended) contains the limitation "said rounded bottom". There is insufficient antecedent basis in the claim (including the limitations of claims 57 and 65, from which claim 71 depends) for this limitation.

15. The previous rejections under 35 U.S.C. 112 (second paragraph) of claims 20, 22-26, 28, 30-34, 36 and 38 are withdrawn in view of the cancellation of that claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

16. Claims 1, 3, 5, 6, 8, 10, 15, 16, 18-20, 22-26, 28, 30-34, 36, 38, 45-50, 57-64, 72-74 and 76-85 rejected under 35 U.S.C. 102(b) as being anticipated by Li (U.S. Patent # 4946800).

Regarding claim 1, Li illustrates (in figures 2, 6 and 7) an integrated circuit (IC) having multiple active circuit components (Figs. 6, 7 and Col. 5 (lines 5-12)) comprising:

a solid substrate 22, 76 of one conductivity type (p);

a solid material pocket 24, 74 of a different conductivity type (n) having a side surface and positioned on a selected top surface of said substrate (see Fig. 2);

a signal-translating, electronic rectifying barrier 25, 71 (pn junction) located between said solid material pocket and the selected top surface of said substrate (see Fig. 2); and

a solid state material region 21, 72 directly contacting said solid substrate (see Fig. 2), said electronic rectifying barrier, and the side surface of said solid material pocket and, together with said electronic rectifying barrier, electrically isolating a selected active circuit element from another neighboring active circuit component to make these two active circuit elements electrically independently operable (see Figs. 2 and 6, 7, Col. 4 (lines 35-40));

said solid state material region having a depth accuracy of better than .13 microns (see claims 1 and 10 of Li) and being continuously and perfectly bonded metallurgically to all said solid substrate, said solid material pocket, and said electronic rectifying barrier, without thermally and electrically insulating voids and microcracks visible at 1000 times magnification in interfacial bonding regions between the bonded device components (Col. 2, lines 30-50 and Col. 12, Lines 50-60);

The claim to the IC being commercially mass-produced is a product by process limitation and lends no patentability to the claim so long as the final product of said

claim is the same as or obvious over the prior art. *In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985). The particular process of mass-production is therefore unpatentable in this device claim given that the final product is anticipated by Li.

While Li specifically discloses the limitation (as seen in the rejection, above), the claim to the depth having an accuracy of better than .13 microns is a product by process limitation and lends no patentability to the claim so long as the final product of said claim is the same as or obvious over the prior art. *In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985). The particular process of forming the depth to a certain degree of accuracy is therefore unpatentable in this device claim given that the final product is anticipated by Li.

Regarding claim 3, Li discloses the integrated circuit as in claim 1, in which said solid material pocket has a specified vertical thickness (see Fig. 2).

The claim to the thickness having an accuracy of less than a few hundred atomic layers is a product by process limitation and lends no patentability to the claim so long as the final product of said claim is the same as or obvious over the prior art. *In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985). The particular process of forming the pocket to a certain degree of accuracy is therefore unpatentable in this device claim given that the final product is anticipated by Li.

Regarding claims 5 and 6, Li discloses the integrated circuit as in claim 1, in which a selected significant portion of a major surface of said solid material pocket (24, 74), said solid state material region (21, 72), and said electronic rectifying barrier (25, 71) gradually and monotonically changes a vertical thickness thereof with closeness in a lateral direction to a lateral edge of said electronic rectifying barrier (see Fig. 2).

Regarding claims 8 and 10, Li discloses the integrated circuit as in claim 1, in which at least a major side surface of said solid material pocket (24) is curved over a major portion thereof (see Fig. 2).

Regarding claims 15 and 16, Li discloses the integrated circuit as in claim 1, in which at least a top major surface of said electronic rectifying barrier (25, 71) is curved (see Fig. 2), and further in which a selected portion of said electronic rectifying barrier (25, 71) has a vertical thickness which gradually increases with closeness in a lateral direction to a lateral edge of said electronic rectifying barrier (see Fig. 2).

Regarding claim 18, Li discloses the integrated circuit as in claim 1. Further, Li discloses in Col. 3, Lines 45-56 that the bottom of the groove can be located 0 microns from the lower end plane of the pn junction, and that the thickness of the junction layer can be 1 micron. Given the structure of Fig. 2, the laterally-extending dimension is therefore inherently less than 1 micron.

Regarding claim 19, Li discloses the integrated circuit as in claim 1, in which:

said solid state material region (21, 72) consists essentially of oxide (Col. 4, Lines 15-20);

said electronic rectifying barrier (25, 71) is a PN junction (Col. 4, Lines 27-32); and

said solid material pocket (24, 74) is of a semiconductor material, Si (Col. 4, Lines 25-30).

Regarding claim 20, Li (in figures 2, 6 and 7) discloses a miniaturized integrated-circuit semiconductor device containing multiple transistors (Figs. 6, 7 and Col. 5 (lines 5-12)) therein, comprising:

a first semiconductor material body (22, 76) having a first polarity (p);

a second semiconductor material body (24, 74) located generally vertically underneath said first semiconductor material body (see Figs. 2 and 7) and having a second polarity that is opposite the first polarity (n);

a signal-translating, electronic rectifying barrier (25, 71) adjoining said first and second semiconductor material bodies (see Figs. 2 and 7); and

a third solid state material body (21, 72) having an electrical conductivity at least one orders of magnitude different from those of said first and second semiconductor material bodies (this property is inherent as silicon is a semiconductor and oxide is an insulator) and directly contacting respective portions of each of said first and second semiconductor material bodies and said

electronic rectifying barrier (see Fig. 2) and, together with said electronic rectifying barrier, electrically isolating a selected transistor in said semiconductor device from another neighboring transistor in the same semiconductor device thereby making these two transistors electrically independently operable (see Figs. 2 and 6, 7, Col. 4 (lines 35-40));

said third solid state material body (21, 72) having two differentially surface-expanded sides that are not parallel to each other (see Fig. 2) to thereby form on said third solid state material body a bottom terminal portion of no more than a micron in thickness in a selected direction (Col. 6, Lines 5-12 and 50-60) (a rounded bottom has a bottom width of zero).

The claim to the IC being commercially mass-produced is a product by process limitation and lends no patentability to the claim so long as the final product of said claim is the same as or obvious over the prior art. *In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985). The particular process of mass-production is therefore unpatentable in this device claim given that the final product is anticipated by Li.

The claim to the thickness having an accuracy of better than a few hundred atomic layers is a product by process limitation and lends no patentability to the claim so long as the final product of said claim is the same as or obvious over the prior art. *In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985). The particular process of forming the thickness to a certain degree of accuracy is therefore unpatentable in this device claim given that the final product is anticipated by Li.

Regarding claim 22, Li (in figures 5, 6 and 7) discloses a miniaturized integrated-circuit semiconductor device containing multiple transistors (Figs. 6, 7 and Col. 5 (lines 5-12)) therein, comprising:

a first semiconductor material body (55) having a first polarity (p);

a second semiconductor material body (54) located generally vertically underneath said first semiconductor material body (see Fig. 5) and having a second polarity that is opposite the first polarity (n);

a signal-translating, electronic rectifying barrier (56) adjoining said first and second semiconductor material bodies (see Fig. 5); and

a third solid state material body (51) having an electrical conductivity at least one orders of magnitude different from those of said first and second semiconductor material bodies (the difference in conductivity is an inherent property of the materials) and directly contacting respective portions of each of said first and second semiconductor material bodies and said electronic rectifying barrier (see Fig. 5) and, together with said electronic rectifying barrier, electrically isolating a selected transistor in said semiconductor device from another neighboring transistor in the same semiconductor device thereby making these two transistors electrically independently operable (see Figs. 5 and 6, 7, Col. 4 (lines 35-40));

said third solid state material body (51) having two differentially surface-expanded sides that are not parallel to each other (see Fig. 5) to thereby form on

said third solid state material body a bottom terminal portion of no more than a micron in thickness in a selected direction (see Fig. 5);

in which said third solid state material body 51 is of an intrinsic semiconductor material (see Fig. 5).

The claim to the IC being commercially mass-produced is a product by process limitation and lends no patentability to the claim so long as the final product of said claim is the same as or obvious over the prior art. *In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985). The particular process of mass-production is therefore unpatentable in this device claim given that the final product is anticipated by Li.

The claim to the thickness having an accuracy of better than a few hundred atomic layers is a product by process limitation and lends no patentability to the claim so long as the final product of said claim is the same as or obvious over the prior art. *In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985). The particular process of forming the thickness to a certain degree of accuracy is therefore unpatentable in this device claim given that the final product is anticipated by Li.

Regarding claim 23, Li discloses the semiconductor device as in claim 20, said third solid state material body (21, 72) has an as-formed metallurgically graded-seal continuity of a graded-seal type with respect to at least one of said first and second semiconductor material bodies (Col. 2, lines 30-50 and Col. 12, Lines 4-10 and 50-60).

Regarding claim 24, Li discloses the semiconductor device as in claim 20, in which the terminal portion of said third solid state material body (21, 72) is vertically within less than a distance from a selected point inside said electronic rectifying barrier; said distance being one micron or .1 microns (Col. 1, Lines 50-60).

Regarding claim 25, Li discloses the semiconductor device as in claim 20, in which said third solid state material body (21, 72) has the same geometry, position, and orientation relative to said first 4 and second 3 semiconductor material bodies, it will allow adequate stress and strain modification on said electronic rectifying barrier (25, 71) thereby improving device performance (Col. 6, Lines 5-12 and 50-60).

Regarding claim 26, Li discloses the semiconductor device as in claim 25, in which said third solid state material body (21, 72) is favorably stressed, and has a blunt and rounded bottom of zero width (Col. 6, Lines 5-12 and 50-60) and in which the rounded bottom of said third solid state material body is located within one micron from a designated point inside said electronic rectifying barrier (Col. 1, Lines 50-60).

Regarding claim 28, Li discloses the semiconductor device as in claim 20, in which said third solid state material body (21, 72) is of an electrically insulating oxide (Col. 4, Lines 15-20).

Regarding claim 30, Li discloses the semiconductor device as in claim 20.

The claim to the thickness having an accuracy of better than .a few hundred atomic layers is a product by process limitation and lends no patentability to the claim so long as the final product of said claim is the same as or obvious over the prior art. *In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985). The particular process of forming the thickness to a certain degree of accuracy is therefore unpatentable in this device claim given that the final product is anticipated by Li.

Regarding claim 31, Li discloses the semiconductor device as in claim 20, in which said third solid state material body (21, 72) has a rounded bottom portion forming an inverted arch (see Fig. 2).

Regarding claim 32, Li discloses the semiconductor device as in claim 20, in which the terminal portion of said third solid state material body (21, 72) is zero in the lateral direction (Col. 6, Lines 5-12 and 50-60).

Regarding claim 33, Li discloses the semiconductor device as in claim 20, in which said electronic rectifying barrier (25, 71) has a curved major surface (see Fig. 2).

Regarding claim 34, Li discloses the semiconductor device as in claim 20, in which said third solid state material body (21, 72) has a cylindrical surface (Col. 9, Lines 15-21).

Regarding claim 36, Li discloses the semiconductor device as in claim 20, in which the electronic rectifying barrier is stressed to improve a performance of said semiconductor device (Cols. 5 and 6, Bridging Paragraph).

Regarding claim 38, Li discloses the integrated circuit as in claim 20, in which:

said solid state material region (21, 72) consists essentially of oxide (Col. 4, Lines 15-20);

said electronic rectifying barrier (25, 71) is a PN junction (Col. 4, Lines 27-32); and

said solid material pocket (24, 74) is of a semiconductor material, Si (Col. 4, Lines 25-30).

Regarding claim 45, Li discloses the integrated circuit as in claim 1, in which said electronic rectifying barrier (25, 71) adjoins both said solid substrate (22, 76) and said solid state material region (21, 72) at a place where a periphery of said electronic rectifying barrier is differentially surface-expanded vertically to passivate the adjoining rectifying barrier (see Fig. 2).

The claims to the barrier being passivated to reduce noise, instability, leakage current, electrical shorts and failure due to low breakdown voltage are purely functional limitations. It is well known that similar structures have similar characteristics and functions. Thus, as the device of Li meets the structural limitations of this claim, it should also exhibit similar functional characteristics.

Regarding claim 46, Li discloses the integrated circuit as in claim 1, in which said solid state material region (21, 72) is less than 1 micron in size/width (Col. 6, Lines 5-12 and 50-60) (rounded bottom) having a bottom of a shape being rounded.

The claim to the size having an accuracy of better than .13 microns is a product by process limitation and lends no patentability to the claim so long as the final product of said claim is the same as or obvious over the prior art. *In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985). The particular process of forming the size to a certain degree of accuracy is therefore unpatentable in this device claim given that the final product is anticipated by Li.

Regarding claim 47, Li illustrates (in figures 5, 6 and 7) an integrated circuit (IC) having multiple active circuit components (Figs. 6, 7 and Col. 5 (lines 5-12)) comprising:

a solid substrate 55 of one conductivity type (p);

a solid material pocket 54 of a different conductivity type (n) having a side surface and positioned on a selected top surface of said substrate (see Fig. 5);

a signal-translating, electronic rectifying barrier 56 (pn junction) located between said solid material pocket and the selected top surface of said substrate (see Fig. 5); and

a solid state material region 51 directly contacting said solid substrate (see Fig. 5), said electronic rectifying barrier, and the side surface of said solid material pocket and, together with said electronic rectifying barrier, electrically isolating a selected active circuit element from another neighboring active circuit

component to make the two active circuit elements electrically independently operable (see Figs. 5 and 6, 7, Col. 4 (lines 35-40));

said solid state material region 51 having a depth accuracy of better than .13 microns (see claims 1 and 10 of Li) and being continuously and perfectly bonded metallurgically to all said solid substrate, said solid material pocket, and said electronic rectifying barrier, without thermally and electrically insulating voids and microcracks visible at 1000 times magnification in interfacial bonding regions between the bonded device components (Col. 2, lines 30-50 and Col. 12, Lines 50-60);

including means for circulating a rapidly moving cooling fluid (52, 57) in a microscopic vicinity of said signal-translating electronic rectifying barrier to achieve surface cooling of said electronic rectifying barrier (see Fig. 5).

The claim to the IC being commercially mass-produced is a product by process limitation and lends no patentability to the claim so long as the final product of said claim is the same as or obvious over the prior art. *In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985). The particular process of mass-production is therefore unpatentable in this device claim given that the final product is anticipated by Li.

While Li specifically discloses the limitation (as seen in the rejection, above), the claim to the depth having an accuracy of better than .13 microns is a product by process limitation and lends no patentability to the claim so long as the final product of said claim is the same as or obvious over the prior art. *In re Thorpe*, 777 F.2d 695, 698, 227

USPQ 964, 966 (Fed. Cir. 1985). The particular process of forming the depth to a certain degree of accuracy is therefore unpatentable in this device claim given that the final product is anticipated by Li.

Regarding claims 48, 49 and 50, Li discloses the integrated circuit as in claim 1, in which a selected portion of a major surface of said solid material pocket (24, 74), said solid state material region (21, 72), and said electronic rectifying barrier (25, 71) gradually and monotonically changes a vertical thickness thereof with closeness in a lateral direction to a lateral edge of said electronic rectifying barrier (see Fig. 2) and is curved.

Regarding claim 57, Li (in figures 2, 6 and 7) discloses a miniaturized, solid-state integrated-circuit semiconductor device containing multiple transistors (Figs. 6, 7 and Col. 5 (lines 5-12)) therein, comprising:

a first solid state material material (22, 76) of a first conductivity type (p);

a second solid state material material (24, 74) of a second conductivity type (n) positioned under the first solid state material (see Figs. 2 and 7), the first and second solid state materials having respective adjoining portions (see Fig. 2);

a signal-translating, rectifying barrier (25, 71) lying between and directly contacting the respective adjoining portions (see Figs. 2 and 7); and

a device material region (21, 72) starting at least in the first solid state material and extending toward the rectifying barrier region to form a lower bottom which is within a micron below a selected point inside the rectifying barrier region to thereby combine with said rectifying barrier region for electrically isolating a selected transistor from another neighboring transistor (see Figs. 2 and 6, 7, Col. 4 (lines 35-40));

a major portion of a top surface area of device chip being occupied by said multiple transistors circuit elements themselves and not by inert or inactive device material regions thereby achieving radically improved, device miniaturization (see Fig. 7).

The claim to the IC being mass-produced is a product by process limitation and lends no patentability to the claim so long as the final product of said claim is the same as or obvious over the prior art. *In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985). The particular process of mass-production is therefore unpatentable in this device claim given that the final product is anticipated by Li.

Regarding claim 58 and 59, Li discloses the integrated circuit as in claim 57, in which:

said rectifying barrier (25, 71) is a PN junction (Col. 4, Lines 27-32); and

the second solid state material (24, 74) is a semiconductor material, Si (Col. 4, Lines 25-30);

the device material region (21, 72) penetrates downward through the rectifying barrier region to reach the second solid state material (24 74) and, in combination with the rectifying barrier region, electrically isolates said multiple transistors from one another (see Fig. 7); and

a bottom of the device material region is closer to zero microns than 0.1 microns below the rectifying barrier region (Col. 3, Lines 50-60).

Regarding claim 60, Li discloses the integrated circuit as in claim 57, in which:

the device material region (21, 72) is an elongated device material region (see Fig. 7); and

consists essentially of oxide (Col. 4, Lines 15-20);

The claim to a dimension having an accuracy of better than a micron is a product by process limitation and lends no patentability to the claim so long as the final product of said claim is the same as or obvious over the prior art. *In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985). The particular process of forming a dimension to a certain degree of accuracy is therefore unpatentable in this device claim given that the final product is anticipated by Li.

Regarding claim 61, Li discloses the integrated circuit as in claim 60, in which a bottom of the elongated device material region (21, 72) is close to zero microns below the rectifying barrier region (Col. 3, Lines 50-60).

Regarding claim 62, Li discloses the integrated circuit as in claim 60, in which the elongated, device material region (21, 72) has an intentionally designed and produced rounded bottom having a vertically curved peripheral surface thereat (see Figs. 2 and 7);

the rectifying barrier region (25, 71) adjoining the rounded bottom of the elongated device material region (21, 72) and having a matching curved peripheral surface thereon thereby passivating and differentially expanding greatly the curved peripheral surface of the rectifying barrier region (25, 71) (see Figs. 2 and 7).

The claims to the barrier being passivated for protection against Type I contaminants, for eliminating wasteful central flat portions at bottoms of similar device material regions in prior art devices, for reducing mismatch thermal stresses leading to electrical device failures, for minimizing electrical field gradient across a surface passivated and expanded, rectifying barrier region, and for improving mechanical and electrical device yields and reliabilities are purely functional limitations. It is well known that similar structures have similar characteristics and functions. Thus, as the device of Li meets the structural limitations of this claim, it should also exhibit similar functional characteristics.

Regarding claim 63, Li discloses the integrated circuit as in claim 57, in which only a minor portion of a top surface area of device chip is not occupied by said multiple transistors themselves (see Figs. 6 and 7);

said multiple transistors having no centrally large and flat oxidized isolation bottoms, thereby achieving device miniaturization (see Fig. 6 and 7 of Li).

Regarding claim 64, Li (in figures 2, 6 and 7) discloses a miniaturized, solid-state integrated-circuit semiconductor device containing multiple transistors (Figs. 6, 7 and Col. 5 (lines 5-12)) therein, comprising:

a second solid state material (22, 76) of a second conductivity type (p);

a first solid state material (24, 74) of a first conductivity type (n) positioned above the first solid state material (see Figs. 2 and 7), the first and second solid state materials having respective adjoining portions (see Fig. 2);

a signal-translating, rectifying barrier (25, 71) lying between and directly contacting the respective adjoining portions (see Figs. 2 and 7); and

a device material region (21, 72) starting at least in the first solid state material and extending toward the rectifying barrier region to form a lower bottom which is within a micron below a selected point inside the rectifying barrier region to thereby combine with said rectifying barrier region for electrically isolating a selected transistor from another neighboring transistor (see Figs. 2 and 6, 7, Col. 4 (lines 35-40));

a major portion of a top surface area of device chip being occupied by said multiple transistors circuit elements themselves and not by inert or inactive

device material regions thereby achieving radically improved, device miniaturization (see Fig. 7);

in which the first solid state material (24, 74) is purposely broken up into a plurality of smaller material patches (see Fig. 7).

The claim to the IC being mass-produced is a product by process limitation and lends no patentability to the claim so long as the final product of said claim is the same as or obvious over the prior art. *In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985). The particular process of mass-production is therefore unpatentable in this device claim given that the final product is anticipated by Li.

The claims to the breaking up of the first solid state material so that mismatch stresses from varying coefficients of material thermal expansions are reduced in proportion to the smaller size of the broken material patches thereby improving device performance are purely functional limitations. It is well known that similar structures have similar characteristics and functions. Thus, as the device of Li meets the structural limitations of this claim, it should also exhibit similar functional characteristics.

Regarding claim 72, Applicant is reminded that intended functional use is given no patentable weight in claims drawn to structure. See In re Pearson 181 USPQ 641 and Ex parte Minks 169 USPQ 120.

Regarding claim 73, Li discloses the integrated circuit as in claim 57, in which the device material region is a vertical and electrically insulating, elongated device material groove (see Figs. 2 and 7); and

a lower end of the vertical, elongated groove has a centrally rounded bottom of substantially zero width in a direction parallel to a top major surface of the second solid state material whereby mismatch stresses in the direction arising from varying coefficients of thermal expansions of different materials in the device are substantially zero in the direction thereby improving device yield, performance, and reliability (see Figs. 1, 2 and 7) (Col. 6, Lines 1-12 and 50-60);

a first selected point on the centrally rounded bottom of said device material reqion having a first non-zero radius of curvature while a second selected point on the centrally rounded bottom of said device material region havinq a second non-zero radius of curvature (Fig. 1, points G and 18);

said first and second radii of curvature differing from each other in a way selected from the group consisting of: a) significantly; b) differing by over several times; 3) differing by over one order of magnitude; and 4) differing by over two orders of magnitude (all of the above apply to the radii of curvature at points G and 18 in Fig. 1 of Li); and

said first and second selected points being both vertically and laterally within one micron of each other (Col. 3, Lines 45-56).

Regarding claim 74, Li discloses the integrated circuit as in claim 57, in which the rectifying barrier region (25, 71) has a curved peripheral surface (see Fig. 2)

The claims to the barrier being curved to achieve enhanced device reliability; increase yield; decreased cost; improved junction surface passivation; increased packing density; increased switching speed; reduced noise, instability, leakage current and electrical shorts; improved breakdown voltage; controlled carriers generation, movement, and recombination at or near the junction region peripheral surface; and regulated optoelectromagnetic interaction of the rectifying barrier region with ambient or contacting material are purely functional limitations. It is well known that similar structures have similar characteristics and functions. Thus, as the device of Li meets the structural limitations of this claim, it should also exhibit similar functional characteristics.

Regarding claims 76 and 77, Li illustrates (in figures 5, 6 and 7) an integrated circuit (IC) having multiple active circuit components (Figs. 6, 7 and Col. 5 (lines 5-12)) comprising:

a solid substrate 55 of one conductivity type (p);

a solid material pocket 54 of a different conductivity type (n) having a side surface and positioned on a selected top surface of said substrate (see Fig. 5);

a signal-translating, electronic rectifying barrier 56 (pn junction) located between said solid material pocket and the selected top surface of said substrate (see Fig. 5); and

a solid state material region 51 directly contacting said solid substrate (see Fig. 5), said electronic rectifying barrier, and the side surface of said solid material pocket and, together with said electronic rectifying barrier, electrically isolating a selected active circuit element from another neighboring active circuit component to make the two active circuit elements electrically independently operable (see Figs. 5 and 6, 7, Col. 4 (lines 35-40));

said solid state material region 51 having a depth accuracy of better than .13 microns (see claims 1 and 10 of Li) and being continuously and perfectly bonded metallurgically to all said solid substrate, said solid material pocket, and said electronic rectifying barrier, without thermally and electrically insulating voids and microcracks visible at 1000 times magnification in interfacial bonding regions between the bonded device components (Col. 2, lines 30-50 and Col. 12, Lines 50-60);

in which a selected round surface of said solid material pocket 54 contacts a non-flat surface on said rectifying barrier 56 (see Fig. 5).

The claim to the IC being commercially mass-produced is a product by process limitation and lends no patentability to the claim so long as the final product of said claim is the same as or obvious over the prior art. *In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985). The particular process of mass-production is therefore unpatentable in this device claim given that the final product is anticipated by Li.

While Li specifically discloses the limitation (as seen in the rejection, above), the claim to the depth having an accuracy of better than .13 microns is a product by process limitation and lends no patentability to the claim so long as the final product of said claim is the same as or obvious over the prior art. *In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985). The particular process of forming the depth to a certain degree of accuracy is therefore unpatentable in this device claim given that the final product is anticipated by Li.

Regarding claim 78, Li discloses the integrated circuit as in claim 1, in which, on a vertical cross-section thereof, two selected points on a bottom major surface of said solid state material region (21, 72) are at two different vertical levels;

said two selected points being both vertically and laterally within one micron of each other (see Fig. 2).

Regarding claim 79, Li discloses the integrated circuit as in claim 1, in which, on a vertical cross-section thereof, two selected points on a bottom major surface of said solid state material region (21, 72) are non-flat but a substantial portion thereof is curved (see Fig. 2);

said two selected points being both vertically and laterally within one micron of each other (see Fig. 2).

Regarding claim 80, Li discloses the integrated circuit as in claim 1, in which, on a vertical cross-section thereof, a specified portion of a selected top major surface and a selected bottom major surface of said solid state material region are non-parallel to a number of said other selected surfaces;

said two selected points being both vertically and laterally within one micron of each other (see Fig. 2).

Regarding claim 81, Li discloses the integrated circuit as in claim 1, in which said solid substrate has a top surface (rounded portion where 21 contacts the solid substrate) that is not parallel to a top surface of said electronic rectifying barrier (see Fig. 2), on a vertical cross-section thereof, a specified portion of a selected top major surface and a selected bottom major surface of said solid state material region are non-parallel to a number of said other selected surfaces;

at least selected portions being within two microns of one another (see Fig. 2).

Regarding claim 82, Li discloses the integrated circuit as in claim 1, in which said rectifying barrier (25, 71) directly contacting said solid state material region has at least a selected portion that is curved (see Fig. 2)

Regarding claim 83, Li discloses the integrated circuit as in claim 1, in which, on a vertical cross-section thereof, selected respective portions of a top major surface of

said solid substrate 22 (portion where feature 21 contacts the substrate is curved), a bottom major surface of said solid material pocket (see Fig. 2), and a top major surface of said rectifying barrier are all curved 25 (portion contacting feature 21);

at least one of three selected curved portions has a first peripheral surface contacting, at a contact area, a second peripheral surface of another of the three selected curved portions (see Fig. 2);

said first peripheral surface being differentially surface-expanded at said contact area over a specified portion thereof (see Fig. 2).

Regarding claim 84, Li discloses the integrated circuit as in claim 1, in which said device material region comprises a cooling fluid (Col. 8, Lines 50-65).

Regarding claim 85, Li discloses the integrated circuit as in claim 1, wherein said solid state material region (21, 72) has a bottom located within 1 micron from a selected point inside said rectifying barrier (Col. 3, Lines 50-60).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims 52-54, 56 and 65-71 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li.

Regarding claim 52, Li illustrates (in figures 4, 6 and 7) an integrated circuit (IC) having multiple active circuit components (Figs. 6, 7 and Col. 5 (lines 5-12)) comprising:

a solid substrate 44, 47, 76 of one conductivity type (p);

a solid material pocket 42, 74 of a different conductivity type (n) having a side surface and positioned on a selected top surface of said substrate (see Fig. 4);

a signal-translating, electronic rectifying barrier 48, 71 (pn junction) located between said solid material pocket and the selected top surface of said substrate (see Fig. 4); and

a solid state material region 41, 72 directly contacting said solid substrate (see Fig. 4), said electronic rectifying barrier, and the side surface of said solid material pocket and, together with said electronic rectifying barrier, electrically isolating a selected active circuit element from another neighboring active circuit component to make these two active circuit elements electrically independently operable (see Figs. 4 and 6, 7, Col. 4 (lines 35-40));

said solid state material region having a depth accuracy of better than .13 microns (see claims 1 and 10 of Li) and being continuously and perfectly bonded metallurgically to all said solid substrate, said solid material pocket, and said electronic rectifying barrier, without thermally and electrically insulating voids and microcracks visible at 1000 times magnification in interfacial bonding regions between the bonded device components (Col. 2, lines 30-50 and Col. 12, Lines 50-60);

in which said solid state material region is an elongated deep and narrow, solid state material region (see Fig. 4 and 6); and including:

a second elongated deep and narrow, solid state material region 46 microscopically close to said elongated deep and narrow, solid state material region (see Fig. 4);

said second elongated, solid state material region having a submicron width or size at a terminal portion thereof where it is closest to said electronic rectifying barrier (rounded bottom); and

both said elongated, solid state material regions being oriented normally of a common major bottom surface of said solid substrate (see Fig. 4), and extending downward from a common top major surface of said solid material pocket whereby said two elongated, solid state material regions region and said second elongated, solid state material region are parallel to each other (see Fig. 4).

The claim to the IC being commercially mass-produced is a product by process limitation and lends no patentability to the claim so long as the final product of said claim is the same as or obvious over the prior art. *In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985). The particular process of mass-production is therefore unpatentable in this device claim given that the final product is anticipated by Li.

While Li specifically discloses the limitation (as seen in the rejection, above), the claim to the depth having an accuracy of better than .13 microns is a product by process limitation and lends no patentability to the claim so long as the final product of said claim is the same as or obvious over the prior art. *In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985). The particular process of forming the depth to a certain degree of accuracy is therefore unpatentable in this device claim given that the final product is anticipated by Li.

Li, however, fails to specifically disclose the distance between each of said two elongated deep and narrow, solid state material regions and said solid substrate and said electronic rectifying barrier; or the aspect ratios of both said elongated, solid state material regions.

It would have been obvious to one of ordinary skill in the art at the time of the invention to make the device of Li smaller, and thus form a device having the dimensions claimed above. The ordinary artisan would have been motivated to modify Li in the above manner for the purpose of increasing the packing density in integrated circuits and increasing the switching speed of the devices (Li, Col. 1, Lines 45-55)

Regarding claim 53, Li discloses the integrated circuit as in claim 52, in which said two elongated, solid state material regions region and said second elongated, solid state material region have different lengths so that these two solid state material regions reach different depths inside said solid substrate (see Fig. 4).

Regarding claim 54, Li discloses the integrated circuit as in claim 52 in which said two elongated, solid state material regions region and said second elongated, solid state material region differ in electrical conductivity by at least one order of magnitude from that of the material of said semiconductor material pocket (the materials disclosed in Li inherently possess this relative property).

Regarding claim 56, Li discloses the integrated circuit as in claim 52 in which:

materials of said two solid material pockets and said solid state material regions are solids which are 100% dense, substantially chemically pure and uniform, and non-contaminating, and impervious to contaminating gases (Col. 6, Lines 20-25);

at least one of said two solid state material regions is stressed to favorably affect a device performance, and has a rounded bottom of zero width so that lateral mismatch stresses at the bottom in the zero width direction is also zero (Col. 6, Lines 1-12 and 50-60),

said electronic rectifying barrier is located within a 1 micron, having a fractional micron accuracy (see claims 1 and 10) from a designated

point inside said electronic rectifying barrier to achieve a beneficial proximity effect (Col. 1, Lines 45-60).

While Li specifically discloses the limitation (as seen in the rejection, above), the claim to the depth having an accuracy of fractional microns is a product by process limitation and lends no patentability to the claim so long as the final product of said claim is the same as or obvious over the prior art. *In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985). The particular process of forming the depth to a certain degree of accuracy is therefore unpatentable in this device claim given that the final product is anticipated by Li.

Regarding claim 65, Li discloses the integrated circuit as in claim 57 (see rejection above), in which the device material region (21, 72) is an elongated, cylindrical (Col. 9, Lines 15-25) device material groove having an aspect ratio of over 3 to 5 (Col. 6, Lines 60-67), and is oriented generally normally of a top major surface of the second solid state material (see Fig. 7).

Li, however, fails to specifically disclose the aspect ratio of the cylindrical device to be over 3 to 5.

It would have been obvious to one of ordinary skill in the art at the time of the invention to make the device of Li smaller, and thus form a device having the dimensions claimed above. The ordinary artisan would have been motivated to modify Li in the above manner for the purpose of increasing the packing density in integrated circuits and increasing the switching speed of the devices (Li, Col. 1, Lines 45-55)

Regarding claim 66, Li discloses the integrated circuit as in claim 65 in which the elongated, cylindrical device material groove (21, 72) is purposely tilted relative to a top surface of the second solid state material so that the device material groove is above a bottom plane of the rectifying barrier region at some places where the groove depth is less than zero (Col. 4, Lines 1-5), substantially coincides with the same bottom plane of the rectifying barrier region at another place where the groove depth is zero, but lies below the same bottom plane of the rectifying barrier region at other places where the growth depth is greater than zero (see Fig. 2).

Regarding claim 67, Li discloses the integrated circuit as in claim 65, in which the device material region (21, 72) is an elongated, cylindrical groove (Col. 9, Lines 15-25) (Col. 6, Lines 60-67).

Li, however, fails to specifically disclose the cylindrical radius to be less than 1 micron.

It would have been obvious to one of ordinary skill in the art at the time of the invention to make the device of Li smaller, and thus form a device having the dimensions claimed above. The ordinary artisan would have been motivated to modify Li in the above manner for the purpose of increasing the packing density in integrated circuits and increasing the switching speed of the devices (Li, Col. 1, Lines 45-55)

Regarding claims 68-71, Li (in figures 4, 6 and 7) discloses a miniaturized, solid-state integrated-circuit semiconductor device containing multiple transistors (Figs. 6, 7 and Col. 5 (lines 5-12)) therein, comprising:

a first solid state material material (44, 47, 76) of a first conductivity type (p);

a second solid state material material (42, 74) of a second conductivity type (n) positioned under the first solid state material (see Figs. 4 and 7), the first and second solid state materials having respective adjoining portions (see Fig. 4);

a signal-translating, rectifying barrier (48, 71) lying between and directly contacting the respective adjoining portions (see Figs. 4 and 7); and

a device material region (41, 72) starting at least in the first solid state material and extending toward the rectifying barrier region to form a lower bottom which is within a micron below a selected point inside the rectifying barrier region to thereby combine with said rectifying barrier region for electrically isolating a selected transistor from another neighboring transistor (see Figs. 4 and 6, 7, Col. 4 (lines 35-40));

a major portion of a top surface area of device chip being occupied by said multiple transistors circuit elements themselves and not by inert or inactive device material regions thereby achieving radically improved, device miniaturization (see Fig. 7);

including at least one additional, elongated, cylindrical device material groove oriented normally of a top major surface of the second solid state material, and microscopically close to the other elongated, cylindrical device material groove 46;

both the two device material grooves having different lengths to thereby extend vertically downward from a common higher, vertical level to different depths into the second solid state material (see Fig. 4) .

in which a bottom of the elongated cylindrical device material groove;

in which the elongated, cylindrical device material groove has said rounded bottom (see Fig. 4); and

the rectifying barrier region 48 adjoins a rounded bottom of the device material groove at a curved peripheral surface thereof, thereby vertically maximizing the peripheral surface expansion and minimizing electrical field gradient across the rectifying barrier region to improve device yield and manufacturability (see Fig. 4).

The claims to the IC being mass-produced and the elongated, cylindrical device material groove being real-time automation controlled to submicron accuracy in a depth to as close to zero microns below the rectifying barrier region as possible, yet still to have a meaningful device yield to be commercially viable because of the submicron depth accuracy are product by process limitations and lend no patentability to the claim so long as the final product of said claim is the same as or obvious over the prior art. *In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985). The particular

process of mass-production is therefore unpatentable in this device claim given that the final product is anticipated by Li.

Li, however, fails to specifically disclose the two device material grooves having sizes of less than two microns, or the groove depth being less than 0.1 microns but microscopically close to zero microns.

It would have been obvious to one of ordinary skill in the art at the time of the invention to make the device of Li smaller, and thus form a device having the dimensions claimed above. The ordinary artisan would have been motivated to modify Li in the above manner for the purpose of increasing the packing density in integrated circuits and increasing the switching speed of the devices (Li, Col. 1, Lines 45-55)

The claims to the barrier being designed specifically for at least one of thermal, magnetic, and electrical contacting or for optical communication to the device, without actual physical exposure to ambient of the second solid state material are purely functional limitations. It is well known that similar structures have similar characteristics and functions. Thus, as the device of Li meets the structural limitations of this claim, it should also exhibit similar functional characteristics.

Response to Arguments

18. Applicant's arguments dated 10/2/2006 have been fully considered but are moot in view of the new grounds of rejection.

Conclusion

19. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to WILLIAM F. KRAIG whose telephone number is (571)272-8660. The examiner can normally be reached on Mon-Fri 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao X. Le can be reached on 571-272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Lex Malsawma/
Primary Examiner, Art Unit 2892

/W. F. K./
Examiner, Art Unit 2892
02/07/2008